Improved electro-thermal simulation of power devices

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Abstract

The purpose of this communication is to present an improved electro-thermal simulation tool, called NASDAC (Non-isothermal Analysis of Semiconductor Devices and Circuits). The simulation code includes all relevant effects, and has been successfully applied to the simulation of complex power silicon bipolar devices. It has been also recently extended to GaAs Heterojunction bipolar transistors (HBT's), and silicon power MOS transistors.

1. Introduction

Electro-thermal simulation of solid-state devices is by no means a trivial task. Several complex factors contribute to the overall electro-thermal behavior. In a previous contribution [1] we presented a first version of our simulation tool which included many important effects:

1) A new efficient analytical approach is used to solve the three-dimensional heat flow equation. This approach is computationally more efficient than numerical approaches such as finite elements, finite differences and thermal networks. This is particularly true in the case of the silicon power bipolar and MOS devices which are presently under investigation, which are composed of an extremely large number of elementary devices (cells). This analytical approach has been recently extended also to multi-layer structures [2].

2) Detailed analytical models are developed to describe the electro-thermal behavior of the elementary devices. It is to be noted that the behavior of power devices can be complicated by effects which do not occur in low power devices (e.g. quasi-saturation in power MOS [3]). As a consequence, electro-thermal models need to be developed specifically for these devices. In [1] we implemented a detailed model for silicon power bipolar transistors. This model has been extended to GaAs HBT's [4], and is presently being extended to power silicon MOSFETs.

3) The simulation code accounts for a finite chip thickness, adiabatic boundary conditions at chip lateral faces and temperature-dependent thermal conductivity.

To validate our code we carried out extensive experimental investigations on the electro-thermal behavior of silicon bipolar power transistors. As shown below, the results of these measurements clearly indicated that two factors strongly influence the device behavior:

1) the cooling effect due to heat conduction through the surface metallization
2) the heat flow across the package under transient conditions.

In this paper we present an improved version of our electro-thermal simulation tool which includes the above factors.

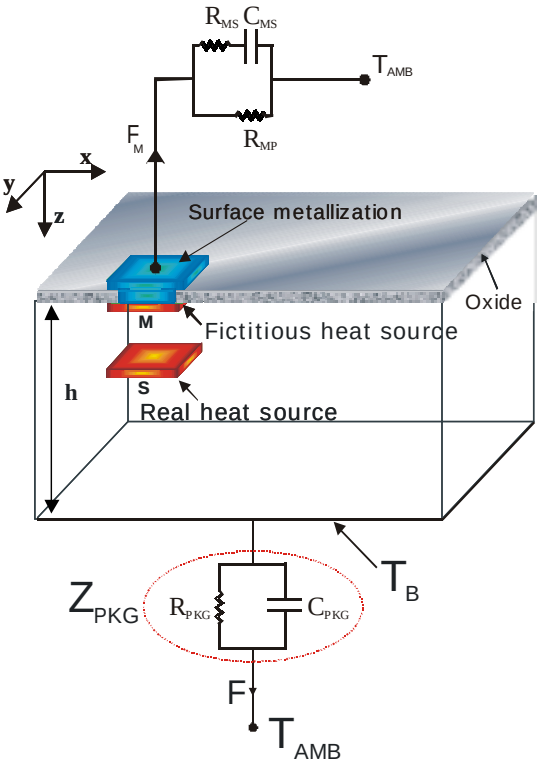

Figure 1. Thermal model of a solid-state device.

The heat flow process across the package has been described by an arbitrarily complex thermal network, which is connected to the bottom surface of the chip (or to the bottom layer in the case of multi-layer structures), assumed to be isothermal. The solution to the mathematical problem of joining the analytical solution of the heat flow equation in the chip to the package thermal

impedance shows that the thermal behavior of the device *cannot* be simply expressed in terms of a series of a thermal impedance related to the chip and a thermal impedance related to the package.

2. Modelling the effect of the package thermal impedance

Heat flow from the bottom of the die to ambient is modeled by means of an arbitrarily complex thermal impedance Z_{PKG}. In general the heat flux F leaving the bottom surface located at z=h (Fig. 1) is time-dependent. This implies that the bottom surface temperature T_B will be also time-dependent. For example, assuming a simple single-pole thermal impedance we have

$$F = \frac{\theta_B}{R_{PKG}} + C_{PKG}\frac{d\theta_B}{dt} \qquad (1)$$

where $\theta_B=T_B-T_{AMB}$ represents the temperature drop across the thermal impedance Z_{PKG}. All other surfaces are assumed adiabatic. In order to take into account boundary condition (1) we express the temperature field as

$$T(\mathbf{r},t) = \theta(\mathbf{r},t) + \theta_1(\mathbf{r},t) + T_{AMB} \qquad (2)$$

The variable $\theta(\mathbf{r},t)$ is defined as the temperature drop with respect to the bottom surface [here $\mathbf{r}$ denotes the position vector $\mathbf{r}=(x,y,z)$]. Since $\theta(\mathbf{r},t)$ is a solution of the time dependent heat flow equation which satisfies a simple isothermal boundary condition at the bottom surface ($\theta=0$), as well as the boundary conditions on the other surfaces, it can be determined by means of the approach outlined in [1] as well as other analytical approaches [5]. The function $\theta_1(\mathbf{r},t)$ is a solution of the heat flow equation which satisfies an isothermal condition $\theta_1=\theta_B(t)$ on the bottom surface and adiabatic conditions on the remaining surfaces. It is readily recognized that this function is dependent only on the *z* variable $\theta_1=\theta_1(z,t)$. Although θ_1 can be easily determined using the classical variable separation method, we did not find this approach very efficient. A more efficient approach can be developed, based on the steady-state solution ($\theta_B(t)$=const.) if the adiabatic condition on the top surface is neglected:

$$\theta_1(z,t) = \theta_B \operatorname{erfc}\left(\frac{h-z}{2\sqrt{\alpha\cdot t}}\right) \qquad (3)$$

In the case of a time-varying temperature $\theta_B(t)$ we have

$$\theta_1(z,t) = \int_0^t \theta_B(\tau)\cdot h(z,t-\tau)d\tau \qquad (4)$$

where h(z,t) represents the time derivative of the erfc function in (3). In order to take into account the adiabatic condition on the top surface the method of images is used, so that the solution θ_1 is actually expressed as a series of image functions obtained by translating (4). This solution is found to require a considerably lower number of terms (typically around 10 for the simulated device) compared to the variable separation method. We are now in the position to calculate the heat flux F leaving the bottom surface:

$$F(t) = F_\theta + F_{\theta_1} = F_\theta(t) + \int_0^t \theta_B(\tau)\cdot\varphi(z,t-\tau)d\tau \qquad (5)$$

where F_θ and $F_{\theta 1}$ are the fluxes related to the solution θ and θ_1, respectively. The latter term is given by a convolution integral similar to (4), while the term F_θ is expressed by a convolution integral involving the power dissipated by the devices [1]. By equating (1) and (5) an integral-differential equation is obtained for the unknown function $\theta_B(t)$. The function $\theta_B(t)$ is found by disctretizing the time variable in finite time steps t_n. In principle $\theta_B(t_n)$ could be simply obtained by discretizing the time derivative in (1) and the integral in (5). This approach, however, requires a small time step t_{n+1}-t_n and hence a large computation time. To solve this problem we have developed an approximate analytical solution of the integral-differential equation for each time interval (t_n,t_{n+1}). This approach, which will be not described in detail for the sake of brevity, has been extended to more complex thermal networks. In particular, a two-pole thermal network (two RC networks connected in series) has been used in the simulations described below.

Finally, we note that the time-varying temperature cannot be simply expressed as $T(\mathbf{r},t)=\theta(\mathbf{r},t)+\theta_B(t)+T_{AMB}$, since $\theta_B(t)$ is not a solution of the heat flow equation. As a consequence, the thermal behavior of the device cannot be simply regarded as a series combination of two thermal impedances, one related to θ and the other one to θ_B (i.e. Z_{PKG}).

3. Modeling of the cooling effect of surface metallization layers

As in most published work, in the previous version of our simulation tool [1] we assumed the top surface to be perfectly adiabatic (i.e. zero heat flux across the surface oxide layer, see Fig. 1). On the other hand, experimental result indicated that power silicon bipolar devices (to be described below) heat loss though the surface metallization plays an important role. The effect of the surface metallization in cooling the surface temperature by removing heat from active areas has been recently investigated in [6]. To model this effect we have developed an approximate, yet simple, approach. For the sake of simplicity let us consider only one active device in the chip represented by heat source S in Fig. 1, and determine the temperature response to a step power. The heat flow F_M through the surface metal contact M is accounted for by connecting the metal contact to an empirical thermal network, including two thermal resistances R_{MS} and R_{MP} and one thermal capacitance C_{MS}. In order to illustrate the approach, we further neglect the thermal capacitance C_{MS} and thermal resistance R_{MS}. Moreover, we assume that the bottom surface is placed on

an ideal heat sink (θ_1=0). In this case the thermal resistance R_{MP} defines the boundary condition

$$F_M = \frac{1}{R_{MP}}(T_M - T_{AMB}) = \frac{1}{R_{MP}}\theta_M \qquad (6)$$

being F_M the heat flux leaving the contact, and θ_M the average surface temperature drop (with respect to ambient temperature) on the metal contact. In order to satisfy the above condition, we introduce a fictitious heat source located on the top surface in correspondence of the metal contact (Fig. 1). The temperature field is the expressed as the superposition of the temperature fields generated by the real and fictitious heat sources: $\theta(\mathbf{r},t)=\theta_{real}(\mathbf{r},t)+\theta_{fict}(\mathbf{r},t)$. Similarly to θ_{real}, the fictitious temperature field θ_{fict} can be calculated by means of the analytical techniques described in [1,2] or [5]. As a result, the average temperature drop θ_M on the metal contact can be expressed as

$$\theta_M(t) = Z_{THreal}(t)P - Z_{THfict}(t)F_M \qquad (7)$$

where the thermal impedances Z_{THreal} and Z_{THfict} define the thermal response to a step power applied to the real and fictitious sources, respectively. The negative sign in the second term in (7) is due to the fact that power F_M is directed outwards. Combining (6) and (7), the unknowns F_M and $\theta_M(t)$ can be determined. In practical cases of multiple heat sources and metal contacts the implementation of this approach becomes considerably more involved. In fact, a fictitious heat source should be assigned to each metal contact, and the overall temperature field is given by the superposition of all real and fictitious fields (including the term $\theta_1(z,t)$.which takes into account the effect of the package impedance). Moreover, in the case of arbitrary transients for the dissipated power P(t), the thermal response must be expressed in terms of convolution integrals. Finally, if the complete thermal network shown in Fig. 1 is considered, the effect of the metallization cannot be described by the simple boundary condition given by (6). A complex algorithm was developed in order to include all of the above factors.

4. Comparison of simulation and experimental results

In order to validate our simulation tool, we investigated the electro-thermal behavior of multicellular power bipolar transistors. Fig. 2 shows the layout of the test pattern considered in the measurements and simulations. The device is composed of 10×10 square emitters surrounded by the base metallization, as shown by the inset in Fig. 2.

The surface temperature of the device was detected under transient conditions using a radiometric detection technique based on an infrared microscope equipped with a cooled InSb sensor [7].

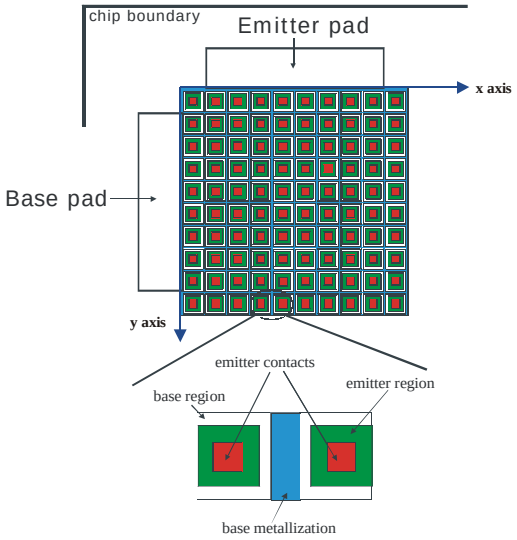

Figure 2. Schematic layout of the power bipolar transistor.

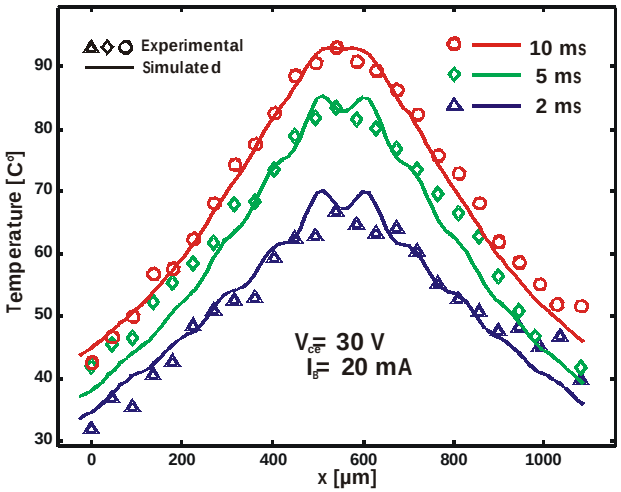

Figure 3. Temperature distribution along the x axis at 2, 5, 10 ms after device turn on (I_B=20 mA, V_{CE}=30 V). Experimental results (symbols) are compared with electro-thermal simulations (full lines).

Fig. 3 shows the temperature distribution along the x axis (in correspondence of the center of the device) at 2, 5, 10 ms after device turn on (with a base current I_B=20 mA and a collector voltage V_{CE}=30 V). It can be clearly noted the formation of a hot spot in the center of the device. Simulated results are in good agreement with experimental data.

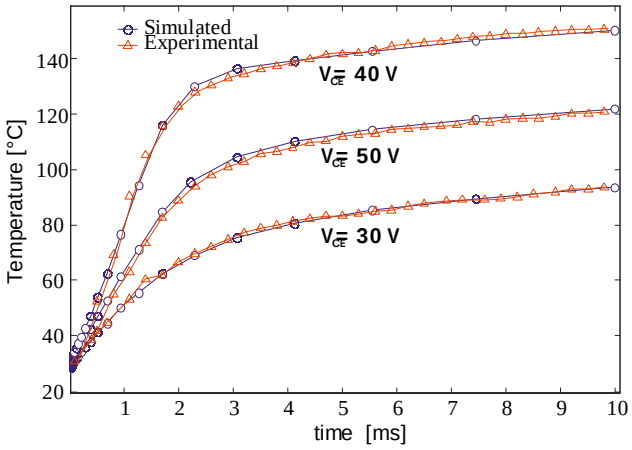

Figure 4. Measured and simulated peak temperature as a function of time for different values of the collector voltage.

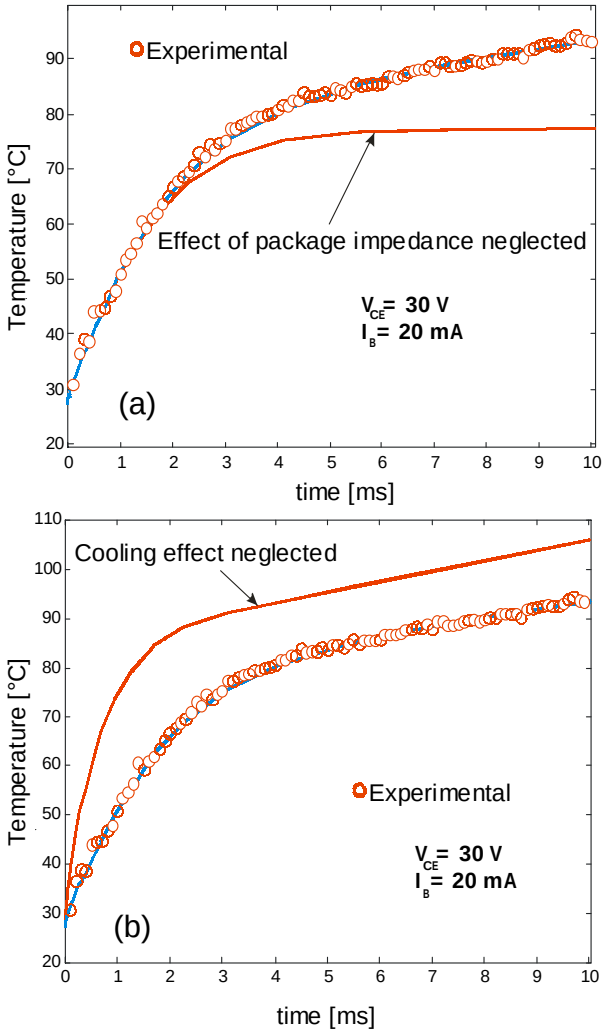

Figure 5. Peak temperature as a function of time.

Fig. 4 shows the measured and simulated peak temperature as a function of time for different values of the collector voltage. The package impedance Z_{PKG} was modelled by means of a two pole network. The effect of the surface metallization was modelled by the full thermal network shown in Fig. 1. In Fig. 5 the same plot is displayed for the case I_B=20 mA and V_{CE}=30 V, showing also the simulated temperature obtained by neglecting the effect of the package impedance (Fig. 5a), and neglecting the cooling effect of the metallization layer (Fig. 5b).

It should be noted that the effect of the package impedance is significant only in the last part of the transient, while surface cooling affects the entire transient. Therefore, the parameters relative to surface cooling thermal network are first determined by fitting the first part of the transient. This leads to the curve shown in Fig. 5a where the effect of Z_{PKG} is not included. Then, the parameters relative to Z_{PKG} can be extracted by fitting the last part of the transient. We are presently investigating improved thermal networks to more accurately model the effect of surface cooling (e.g. reduction of the surface temperature gradient due to heat spreading [6]).

References

[1] M. Macchiaroli, N. Rinaldi, V. d'Alessandro, G. Breglio and P. Spirito, "A new electro-thermal simulation tool for the analysis of bipolar devices and circuits," *IEEE Therminic2001 Conf.*, Paris, 2001.

[2] N. Rinaldi, "Generalized image method with application to the thermal modelling of power devices and circuits", *IEEE Transactions on Electron Devices*, vol. 49, pp. 679-686, 2002.

[3] V. d'Alessandro, F. Frisina, N. Rinaldi, "A new SPICE model of VDMOS transistors", *EPE2001 Conf.*, session DS2.1, Graz.

[4] M. Macchiaroli, V. d'Alessandro e N. Rinaldi, "NASDAC – A new simulation tool for the electro thermal analysis of bipolar devices: application to multi-finger AlGaAs/GaAs HBT's", MIEL 2002 Conference.

[5] W. Batty, C. Christoffersen, S. David, A. Panks, R. Johnson, C. Snowden, and M. Steer, "Fully physical time-dependent compact thermal modelling of complex non linear 3 dimensional systems for device and circuit level electro-thermal CAD", *IEEE SEMI-THERM Symp.*, p. 71, 2001.

[6] C. Reimer, T. Smy, D. Walkey, B. Beggs, and R. Surridge, "A simulation study of IC layout effects on thermal management of die attached GaAs ICs", *IEEE Trans. On Comp. And Packaging Tech.*, 23, p. 341, 2000.

[7] G. Breglio, S. Pica, and P. Spirito, "Thermal effects and electro-thermal modeling in power bipolar transistors", *MIEL97 Conf. Proc.*, Nis, 1997.